

# Pulse-Driven Josephson Digital/Analog Converter

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**Abstract**— The authors have designed and demonstrated a pulse-driven Josephson digital/analog converter. When used as a programmable voltage standard, this device can synthesize metrologically accurate ac waveforms as well as stable dc voltages. We show through simulations that Josephson quantization produces a nearly ideal quantization noise spectrum when a junction is driven with a typical waveform produced by a digital code generator. This technique has been demonstrated in preliminary experiments with arrays of 1000 junctions clocked at frequencies up to 6 Gb/s, where sine waves of a few millivolts in amplitude were synthesized at frequencies up to 1 MHz.

**Index Terms**— Array, D/A converter, digital/analog converter, Josephson, Josephson junction, pulse, quantization, superconductor, voltage standard.

## I. INTRODUCTION

THE National Institute of Standards and Technology (NIST) is developing Josephson digital/analog (D/A) converters as fast programmable voltage standards for the following applications: 1) calibration of dc reference standards and digital voltmeters; 2) characterization of commercial D/A and A/D converters; and 3) generation of digitally synthesized ac waveforms with calculable root mean square (rms) voltages. In the last application, primary standards for ac voltage presently rely on thermal voltage converters that compare the heating effect of ac and dc inputs. Direct waveform synthesis from a Josephson source would provide an independent method for making ac measurements and for determining the accuracy of thermal voltage converters.

In 1995 Hamilton *et al.* proposed a Josephson D/A converter based on a binary sequence of series arrays of resistively shunted tunnel junctions [1]. When biased with a microwave frequency  $f$ , each junction exhibits constant voltage steps at  $V = n\hbar/K_J$ . The Josephson frequency-to-voltage ratio  $K_J = 483\,597.9$  GHz/V is a defined constant that is approximately  $2e/h$ , where  $h$  is Planck's constant and  $e$  is the elementary charge. The quantum step number  $n = -1, 0$ , or  $+1$ , corresponds to the number and polarity of junction pulses per period  $1/f$  and is determined by the array bias. The average dc voltage of each array of  $N$  junctions is

$$V = nN\hbar/K_J. \quad (1)$$

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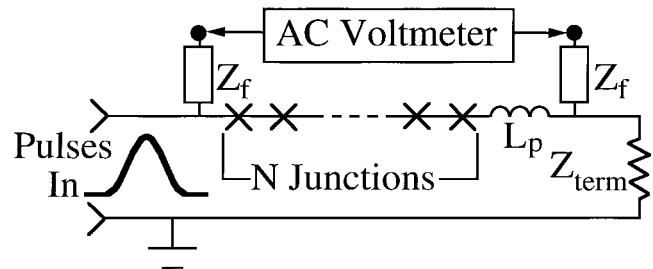


Fig. 1. Josephson array pulse quantizer for a D/A converter.

Different output voltages are programmed by using independent bias currents to select the voltage of each array segment in the binary series, for which  $N = 1, 2, 4, \dots, 16\,384$ .

To improve the performance of these arrays, NIST has developed a superconductor-normal-super conductor (SNS) trilayer junction technology [2], [3]. These SNS junctions have large critical currents,  $I_c > 1$  mA, that provide higher output current and better stability against noise. Their internal resistance results in a nonhysteretic current-voltage curve that is inherently stable without the use of external shunt resistors. This junction technology and circuit design has advanced to the level where a binary sequence circuit with 32 768 SNS junctions in nine independently selectable arrays on a single chip has demonstrated stable accurate voltages over the range from  $-1.2$  to  $+1.2$  V [2]–[6]. This circuit is already being used in applications where perfectly stable and programmable dc voltages are required.

Although the binary-sequence design is adequate for *fast* programming of *dc* voltages, in the first two applications listed above, it has not proved practical for generating *fast* ac waveforms. Switching the bias of selected arrays produces switching transients that result in a substantial uncertainty in the generated waveform [7]. However, instead of changing the quantum number  $n$  or number of junctions  $N$ , the output voltage can also be controlled by changing the excitation frequency  $f$ . Recently, we have shown that if a pulse excitation is used instead of a sine wave, the step amplitude is independent of the pulse repetition frequency for all frequencies below a characteristic frequency  $f_c = I_c R K_J$ , where  $R$  is the junction's normal state resistance [8], [9].

## II. VOLTAGE PULSE QUANTIZATION

As shown in Fig. 1, a pulse-driven Josephson D/A converter consists of a single large array of  $N$  junctions distributed along a wide bandwidth transmission line. When a pulse propagates down the line, it induces a quantized voltage pulse with a time-

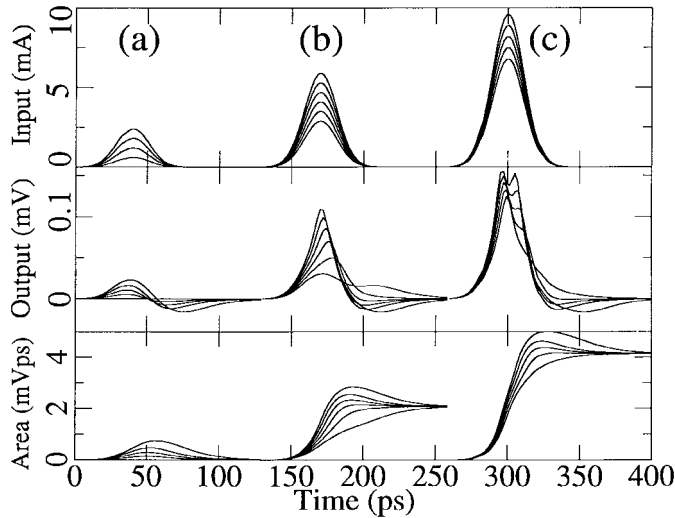


Fig. 2. Input current (top), junction voltage (middle), and time integral of the junction voltage (bottom) for a pulse driven Josephson junction, illustrating quantization of the junction voltage. Peak input amplitudes range from: (a) 0–2.4 mA (5 lines), (b) 2.9–5.9 mA (6 lines), and (c) 6.8–9.6 mA (5 lines).

integrated area  $n/K_J$  across each junction it passes. As in (1),  $n$  is an integer that corresponds to the number of junction pulses for each input pulse. Thus a pulse train of frequency  $f$  propagating down the line generates an average voltage  $nNf/K_J$  across the array. A complex output waveform can be generated by gating the input pulse train with a long digital word generator. A knowledge of the digital code, the clock frequency, and the number of junctions in the array is sufficient to precisely calculate the output waveform. Since there is only one array, the uncertainty associated with switching between arrays is eliminated and the number of Josephson pulses occurring in any time increment is calculable.

The pulse quantizing behavior of a Josephson junction can be readily understood by the numerical simulation of a resistively shunted junction model. Fig. 2 shows a sequence of current inputs applied to a single junction (top), the junction voltage (middle), and the time integral (area) of the voltage pulses (bottom). The three sets of input current pulses (a)–(c) each span a peak amplitude range that corresponds to the quantum integers  $n = 0, 1$ , and  $2$ . For example, for the current range from 2.9 to 5.9 mA in Fig. 2(b), the junction generates exactly one voltage pulse for each input pulse corresponding to  $n = 1$  quantization. The shape of this voltage pulse varies with the input current pulse amplitude, but its time integral is exactly  $1/K_J$ . In a series array of  $N$  junctions the voltages across all junctions add. If the input current pulse amplitude is in the range that generates just one output pulse for each junction, then the output pulse time integral is exactly  $N/K_J$ .

Fig. 3 is a block diagram of the process that is used to synthesize a desired sine wave of frequency  $f$  or any other periodic waveform from quantized Josephson pulses. The process begins with the modulator algorithm block, a computer program that digitizes  $m$  periods of an input sine wave  $S(t)$  at a sampling frequency  $f_s$ . A two-level modulator with spacing  $\Delta$  generates  $mN_s$  two-state ( $-\Delta/2$  or  $+\Delta/2$ ) digital samples, where  $N_s = f_s/f$  is the number of samples per period. The

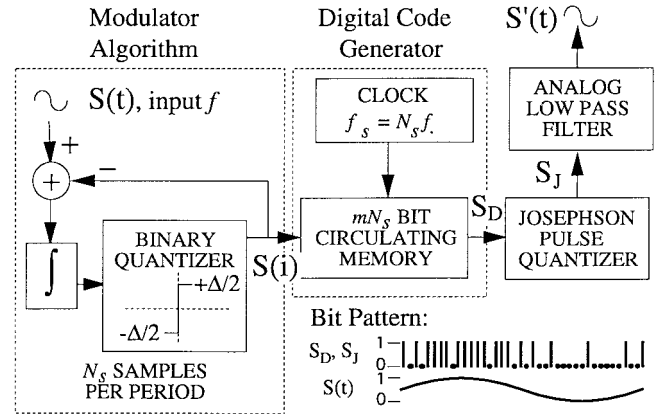


Fig. 3. A block diagram of a delta-sigma digital-to-analog converter based on pulsed Josephson junctions.  $S(t)$  is the desired waveform and  $S'(t)$  is the output waveform.

modulator output  $S(i)$  is therefore a long digital sequence where the density and sign of the levels are proportional to the input. The Fourier spectrum of the resulting output code  $S(i)$  consists of the desired waveform plus additional harmonics of  $f$  (and  $f/m$  for  $m > 1$  period) that are known as quantization noise. We chose a particular modulator called a second-order delta-sigma modulator that uses a quantizer (delta modulator), an integrator (sigma), and feedback of the quantized signal to minimize the output quantization noise and thereby increases the signal-to-noise ratio and dynamic range over a desired frequency band  $f_o$  [10]. Specifically, we used a second-order delta-sigma modulator (not shown) with two feedback paths and two integrators that provides a total rms quantization noise in the signal band given by  $n_o \approx 1.27\Delta (\text{OSR})^{-5/2}$ , where  $\text{OSR} = f_s/(2f_o)$  is the oversampling ratio.

For a repetitive waveform, the modulator generated code is calculated just once and stored in the circulating memory of the digital code generator. The digital code generator recreates the waveform as an output voltage in real time  $S_D(t)$  by clocking the memory at the sampling frequency. Each output digit generates either a negative or a positive current pulse that is launched into the Josephson array stripline. The Josephson array quantizes the time integral of the pulses producing a time-dependent analog output voltage  $S_J(t)$ . The modulator signal bandwidth  $f_o$  is chosen larger than the low-pass filter bandwidth. Since most of the quantization noise occurs at frequencies far above  $f_o$ , a low-pass filter can eliminate it, leaving only the desired waveform  $S'(t) \approx S(t)$ . Systems like that shown in Fig. 3 (without the Josephson pulse quantizer) that generate analog signals by summing many pulses are called delta-sigma D/A converters.

In order to produce a bipolar ac voltage, the Josephson array requires both positive and negative pulses. This requires  $S_D(t)$  to be a three-level voltage input pattern with a 0-V level in between the  $+\Delta$  high level and  $-\Delta$  low level of bit pattern  $S(i)$ . In our present experiments we use a two-level voltage output pattern, which allows the creation of only unipolar output waveforms. An example of a simple two-level bit pattern for creating a unipolar sine wave is shown in the inset of Fig. 3.

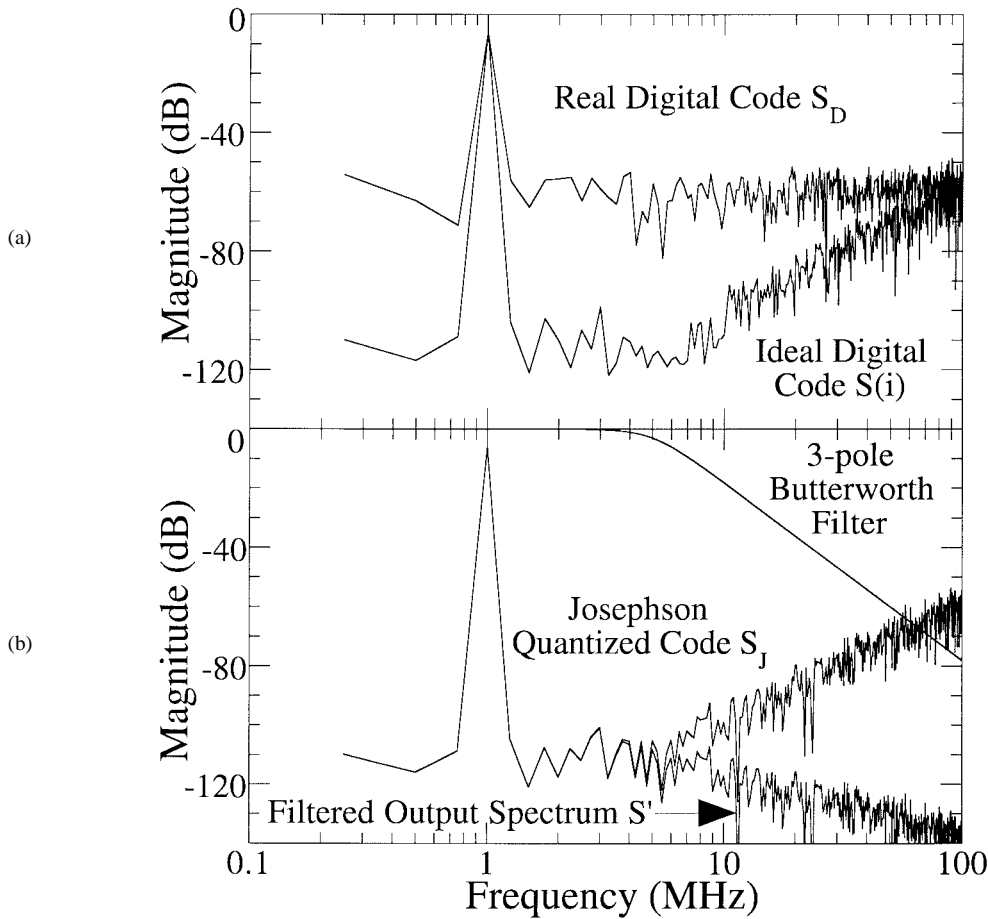


Fig. 4. The simulated Fourier spectra of the signals in the Josephson delta-sigma D/A converter. (a) Spectra of input codes prior to Josephson quantizer and (b) spectra of Josephson quantized output waveforms.

Next we demonstrate why the Josephson quantizer is an essential component of an accurate D/A converter by considering the Fourier spectra of the intermediate waveforms in Fig. 3. Consider a 1-MHz unipolar sine wave with peak amplitude  $V_p = \Delta/4$ , having  $m = 4$  periods and sampled at 2.56 GHz. Since the sine wave is generated by repeating the digital sequence indefinitely, the Fourier transform of the digital code  $S(i)$  is a line spectrum with a dominant line at  $f = 1$  MHz. The line spectrum for this “ideal digital code” is shown in Fig. 4(a), where for clarity we have connected the points representing the power in each harmonic. The peak at 1 MHz is the desired sine wave signal, and all of the other lines are quantization noise. The oversampling ratio of the delta-sigma modulator is 128. This produces a modulator signal bandwidth of 10 MHz within which the quantization noise of all harmonics are at least 100 dB below the signal frequency.

If we could directly generate this perfect digital code, then there would be no need for the Josephson array because a perfect digital code is quantized by definition. However, the output  $S_D$  of typical digital code generators has amplitude and phase distortion. When we recompute the spectrum including realistic values for the amplitude and phase distortion (normal distributions with  $\sigma = 2.5\%$ ) that is uncorrelated with the input sine wave, the result is the “real digital code” curve.

The quantization noise within the modulator signal band has increased about 50 dB over the ideal digital code so that the spectrum is not sufficiently calculable to be useful for metrology.

Next we bias a Josephson junction (or array) with this real digital code. We use the optimum pulse width,  $\tau = (2f_c)^{-1}$  [8]. The junction equations are integrated to find the periodic solution [11], resulting in the junction output voltage  $S_J(t)$ . The corresponding “Josephson quantized code” spectrum in Fig. 4(b) is almost identical to the ideal digital code spectrum. *Thus, even though the Josephson array does nothing to improve time jitter and it does not quantize the pulse amplitudes, the fact that the time integral of the pulses is quantized is sufficient to produce a nearly ideal spectrum.* The effect of the amplitude and phase distortion in the input digital code and random variations in junction parameters is to reduce the current bias margin of the circuit and reduce the current that can be supplied to a load.

Fig. 4(b) also shows the result when  $S_J(t)$  is filtered by a three-pole Butterworth transfer function with a 5-MHz cutoff frequency. The resulting final output waveform  $S'(t)$  is shown as the “filtered output spectrum.” The Butterworth cutoff frequency is chosen to be one-half of the 10-MHz modulator signal bandwidth so that the filtered output spectrum rolls off with increasing frequency. Under these conditions, uncertainty

in the filter cutoff frequency does not significantly affect the accuracy of the final output voltage.

In metrology applications we wish to generate a pure sine wave with a large signal-to-noise ratio but, in particular, the smallest possible uncertainty in the rms signal voltage  $V_o$ . The contribution to the rms voltage of the quantization noise in the filtered signal  $S'(t)$  is the uncertainty of interest. If we assume that the total in-band quantization noise of the Josephson quantized signal is approximately the same as that for the ideal code, then the uncertainty in the rms voltage of the synthesized sine wave is  $U \approx n_o^2/(2 V_o^2) = 1.62 (\text{OSR})^{-5} (\Delta/V_p)^2$  [10]. One can therefore choose an appropriate oversampling ratio for a desired uncertainty and output voltage. Uncertainty less than one part in  $10^7$  can be achieved using second-order delta-sigma modulation for synthesized sine waves with peak amplitude  $V_p \geq 0.1(\Delta/2)$  by choosing an oversampling ratio greater than or equal to 92. For example, such sine waves with frequencies up to a modulator band width of 30 MHz can be generated with a digital code generator having a 6-GHz sampling frequency. In the example of Fig. 4 where  $\text{OSR} = 128$ , the quantization noise increases the rms voltage by only one part in  $10^9$ .

In other simulations, Josephson quantization reduces the quantization noise from digital codes having realistic values of voltage and phase distortion that are correlated to the bit pattern, similar to the uncorrelated case above. However, both correlated and uncorrelated distortion may introduce harmonics in the filter bandpass whose magnitude Josephson quantization does not fully reduce to that of the ideal digital code. Nevertheless, with appropriate modulator design and oversampling ratio, present technology is capable of synthesizing sine waves at frequencies below 30 MHz with uncertainty less than one part in  $10^7$ . In practice, other effects, such as common mode rejection or electromagnetic coupling between input and output, will dominate the uncertainty of the output voltage.

### III. EXPERIMENTAL RESULTS

In order to demonstrate these ideas, we have designed and fabricated a circuit consisting of a 7-mm-long array of 1000 junctions along the center conductor of a 50- $\Omega$  superconducting coplanar stripline [3], [9]. The stripline is terminated by a 50- $\Omega$  resistor and connections to the ends of the array are made through low-pass filters. Equation (1) shows that the maximum voltage range of this test circuit is only a few millivolts. This is sufficient for our feasibility study, but much larger circuits with up to 100 000 junctions will be required for practical D/A converters.

Fig. 5 is a preliminary experimental verification of the theoretical results of Fig. 4. In this experiment we synthesize one period of a 23.4-kHz sine wave using a 256-kb code and a 6-GHz clock frequency. The sine wave is unipolar with a peak-to-peak amplitude of 4.3 mV. The digital code is generated by a second-order delta-sigma modulator algorithm with an oversampling ratio of 256. In the absence of noise or jitter, this ideal code yields harmonics at least 100 dB below the fundamental for all frequencies below 50 MHz.

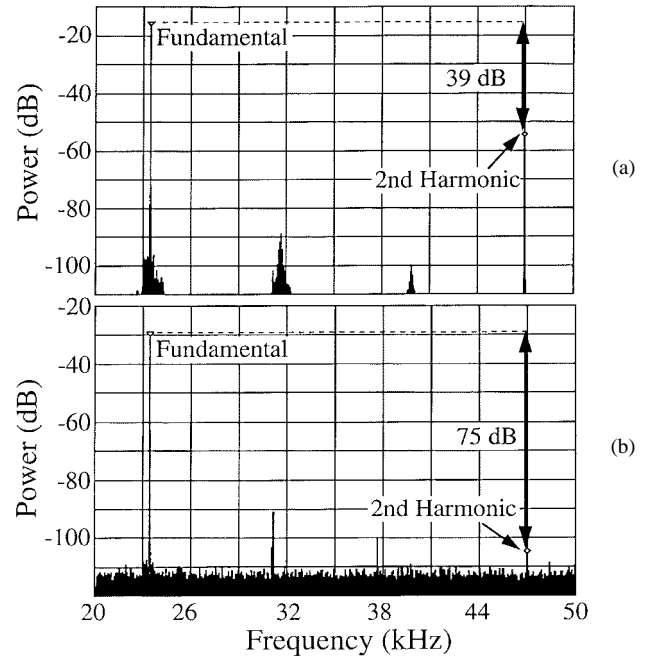


Fig. 5. Measured Fourier spectra showing that the quantizing effect of the array improves signal purity. (a) Digital code generator spectrum and (b) amplified spectrum of Josephson array voltage. Both spectra are taken with a 1-Hz resolution bandwidth and a 1-Hz video bandwidth. The unlabeled signals are spurious.

However, the output spectrum of the digital code generator, shown in Fig. 5(a), shows the measured power in the second harmonic is only 39 dB below the fundamental. The large second harmonic as well as large higher harmonics (not shown) are caused by voltage levels of the digital code that are correlated with the density of 1's. The spectrum of the corresponding amplified Josephson array output is shown in Fig. 5(b). For the Josephson array output, the difference between the fundamental and second harmonic is 75 dB. Comparison of spectra (a) and (b) shows that the Josephson array circuit has reduced the nonideal harmonics by about 36 dB. Similar harmonic reduction is obtained for signal frequencies of 2.34 and 234 kHz.

This experimental result verifies that the quantizing effect of Josephson junctions will greatly reduce particular types of distortions inherent in the output of conventional digital code generators. However, the second harmonic, at 75 dB below the fundamental, is still 25 dB greater in amplitude than expected. The most probable reason for this discrepancy is electromagnetic coupling of the input digital code signal to the output leads, either on the chip or at the chip end of the probe where signals are launched on and off the chip. Other sources of measurement uncertainty are discussed below.

### IV. UNCERTAINTY IN THE MEASURED AC VOLTAGE

We have established that a Josephson junction biased with a conventional digital code generator can generate voltage waveforms in which the quantization noise contribution to the rms output voltage is on the order of one part in  $10^9$ . There is, therefore, the potential to develop an ac voltage source with an uncertainty at least 100 times better than the state of the art in

ac voltage measurements, particularly at megahertz frequencies [12]. However, there are several sources of uncertainty in the voltage measured by an ac voltmeter external to the cryostat that challenge the attainability of this uncertainty and constrain the design of the ac voltage standard measurement circuit.

The design of the passive components  $Z_f$  and  $Z_{\text{term}}$  in Fig. 1 is critical in order to achieve the lowest possible uncertainty in the measurement of the generated voltage  $V_{\text{out}}$ .  $Z_{\text{term}}$  is required to eliminate pulse reflections at the end of the line. Any such reflections result in nonuniform input pulse coupling to the junctions along the line. If the input pulse amplitude for any junction falls outside the quantization margins illustrated in Fig. 2, then the output amplitude is no longer calculable. However,  $Z_{\text{term}}$  also generates an error in the measured voltage through the voltmeter's finite common mode rejection ratio (CMRR). In earlier experiments, the common mode voltage at the signal frequency generated by  $Z_{\text{term}}$  was more than 100 times greater than the signal  $V_{\text{out}}$  generated by the junctions. Thus, to achieve a one part in  $10^6$  uncertainty in the measurement of  $V_{\text{out}}$ , the voltmeter would have needed a CMRR of greater than 160 dB—a most unreasonable requirement. The 1000 junction test circuit has been designed to reduce these common mode voltages to below the signal voltage amplitude. Further improvements are required, particularly for higher signal frequencies where the CMRR of voltmeters is lower.

A second challenge is to design the output filters  $Z_f$  at either end of the array. These filters need to have a high impedance at the clock frequency so as not to disturb the input pulses, and they must be a low impedance at the signal frequency so as not to attenuate the signal output. Achieving the required broadband response, within the constraints of planar integrated circuit design, is a considerable challenge.

In addition to the junctions, the coplanar transmission line also has a distributed inductance represented schematically by a lumped inductance  $L_p$  in Fig. 1. The spectrum of the pulse train contains a strong component at the signal frequency, and this component induces an unwanted voltage across  $L_p$ . While this voltage is in quadrature with the signal voltage, it still contributes a significant error at frequencies above 10 kHz. Similarly, stray capacitive or inductive coupling between the input pulse train and the output leads contributes another source of uncertainty in the output voltage. These effects, however, can be measured and corrected because they add a component to  $V_{\text{out}}$  that varies quadratically with the input pulse amplitude. (Over the normal range of operation, the junction contribution to  $V_{\text{out}}$  is independent of input pulse amplitude.) The series inductance contribution to the quadrature voltage at the signal frequency can be estimated for the 1000 junction test circuit. Estimating a 3-mA peak-to-peak input current through the 3-nH inductor at the 23.4 kHz signal frequency yields an error in the 4.3-mV peak-to-peak quadrature output voltage of five parts in  $10^8$ . For 234 kHz, the error is 100 times larger.

Another significant uncertainty component arises from the effects of attenuation and reflection in the coaxial cable to the ac voltmeter. AC voltage metrology traditionally minimizes

this uncertainty by using short lengths of cable and by defining a plane where the ac voltage is known. For our prototype pulse-driven array standard the defined ac voltage is on a chip at one end of a probe inside a liquid helium Dewar. The probe for the present experiments used a 1-m-long coaxial cable. The magnitude of the errors that result depend on the type of cable, its length, the signal frequency, and the quality of the connectors used. As an example, the error in the 1-MHz signal voltage measured by an ac voltmeter with a high input impedance is approximately  $500 \times 10^{-6}$  for a 1-m length of RG-58 coaxial cable with perfect connectors. Since the error is proportional to the square of the length, it could be reduced by two orders of magnitude by using a probe and helium cryostat designed to allow the use of 0.1 m cable length.

## V. CONCLUSIONS

Implementations of Josephson voltage standards prior to this work use a fixed frequency to trigger quantized junction pulses that are averaged into a dc voltage. In this paper we demonstrate how a complex pattern of pulses driving an array of 1000 junctions produces a smooth sine wave output with high resolution and accuracy. Efforts are underway to increase the number of junctions and the clock frequency to achieve a voltage range of  $\pm 1$  V. Success in this effort will lead to a new programmable Josephson voltage standard that can produce quantum mechanically accurate dc and ac voltages with a frequency range from 0 to 30 MHz.

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## REFERENCES

- [1] C. A. Hamilton, C. J. Burroughs, and R. L. Kautz, "Josephson D/A converter with fundamental accuracy," *IEEE Trans. Instrum. Meas.*, vol. 44, pp. 223–225, Apr. 1995.
- [2] S. P. Benz, "Superconductor-normal-superconductor junctions for programmable voltage standards," *Appl. Phys. Lett.*, vol. 67, pp. 2714–2716, Oct. 1995.
- [3] S. P. Benz and C. J. Burroughs, "Constant voltage steps in Nb–PdAu–Nb Josephson junction arrays," *IEEE Trans. Appl. Supercond.*, vol. 7, pp. 2434–2436, June 1997.
- [4] C. A. Hamilton, S. P. Benz, C. J. Burroughs, and T. Harvey, "SNS programmable voltage standard," *IEEE Trans. Appl. Supercond.*, vol. 7, pp. 2472–2474, June 1997.
- [5] C. A. Hamilton, C. J. Burroughs, and S. P. Benz, "Josephson voltage standards: A review," *IEEE Trans. Appl. Supercond.*, vol. 7, pp. 3756–3761, June 1997.
- [6] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, and L. A. Christian, "Stable 1 V programmable voltage standard," *Appl. Phys. Lett.*, vol. 71, pp. 1866–1868, Sept. 1997.
- [7] C. A. Hamilton, C. J. Burroughs, S. P. Benz, and J. R. Kinard, "AC Josephson voltage standard: Progress report," *IEEE Trans. Instrum. Meas.*, vol. 46, pp. 224–228, Apr. 1997.
- [8] S. P. Benz and C. A. Hamilton, "A pulse-driven programmable Josephson voltage standard," *Appl. Phys. Lett.*, vol. 68, pp. 3171–3173, May 1996.
- [9] S. P. Benz, C. J. Burroughs, and C. A. Hamilton, "Operating margins for a pulse-driven programmable voltage standard," *IEEE Trans. Appl. Supercond.*, vol. 7, pp. 2653–2656, June 1997.
- [10] S. R. Norsworthy, R. Schreier, and G. C. Temes, Eds., *Delta-Sigma Data Converters: Theory, Design, and Simulation*. New York: IEEE Press, 1997.

- [11] K. Wiesenfeld, S. P. Benz, and P. A. A. Booi, "Phase-locked oscillator optimization for arrays of Josephson junctions," *J. Appl. Phys.*, vol. 76, pp. 3835–3846, Sept. 1994.
- [12] M. Klonz, "CCE comparison of ac–dc voltage transfer standards at the lowest attainable level of uncertainty," *IEEE Trans. Instrum. Meas.*, vol. 46, pp. 342–346, Apr. 1997.



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